What is claimed is:

1. A circuit for generating dot clock pulses for driving a light-emitting element employed in an optical-writing section of an image-forming apparatus, comprising:

a digital-delay dot clock adjusting section to adjust timings of rising-edges or falling-edges of said dot clock pulses generated by changing a selection for a plurality of delayed-clock pulses, which are generated by delaying clock-pulses, outputted from a reference oscillator, in slightly different delay times; and

a controlling section to control a selecting operation for said plurality of delayed clock pulses, performed in said digital-delay dot clock adjusting section, so as to compensate for unevenness of scanning-light amount caused by an optical element employed in said optical-writing section.

2. A circuit for generating dot clock pulses for driving a light-emitting element employed in an optical-writing section of an image-forming apparatus, comprising:

an index sensor to detect a light-beam, which is emitted from said light-emitting element and is deflected for scanning by a light-scanning device employed in said optical-

writing section, and to output an index signal when said index sensor detects said light-beam at an end portion of a main-scanning region scanned by said light-beam;

a delay-chain section to generate a plurality of delayed-clock pulses by delaying clock-pulses, outputted from a reference oscillator, in slightly different delay times;

a synchronized clock pulse detecting section to select synchronized delayed-clock pulses, which are synchronized with said index signal, out of said plurality of delayed clock pulses generated in said delay-chain section, and to output a number of delay-stages, which is derived from said synchronized delayed-clock pulses, as synchronizing information;

a table memory to store scanning-light unevenness information, which represents unevenness of scanning-light amounts caused by an optical element employed in said optical-writing section;

a delayed-clock switching section to generate a select signal, for selecting a specific delayed-clock pulse, having a phase suitable for compensating for said unevenness of scanning-light amount caused by said optical element employed in said optical-writing section, out of said plurality of delayed-clock pulses, based on said synchronized delayed-

clock pulses and said synchronizing information outputted from said synchronized clock pulse detecting section and said scanning-light unevenness information stored in said table memory; and

a selector to select said specific delayed-clock pulse out of said plurality of delayed-clock pulses in response to said select signal generated by said delayed-clock switching section.

3. The circuit of claim 2,

wherein said select signal is generated in said delayed-clock switching section by performing a calculating operation, based on said synchronized delayed-clock pulses outputted by said synchronized clock pulse detecting section and said scanning-light unevenness information stored in said table memory.

4. The circuit of claim 2,

wherein said select signal is generated in said delayed-clock switching section by performing a table-converting operation, based on said synchronized delayed-clock pulses outputted by synchronized clock pulse detecting

section and said scanning-light unevenness information stored in said table memory.

5. The circuit of claim 2,

wherein said unevenness of scanning-light amount is a variation of light amount due to non-uniformity of reflectance and/or transmittance caused by said optical element.

6. The circuit of claim 2,

wherein said delay-chain section, said synchronized clock pulse detecting section, said table memory and said selector are digital circuits fabricated in an integrated circuit.

7. An image-forming apparatus, comprising:

an image-forming section that includes an optical-writing section to form an image; and

a circuit for generating dot clock pulses for driving a light-emitting element employed in said optical-writing section included in said image-forming section;

wherein said circuit includes,

a digital-delay dot clock adjusting section to adjust timings of rising-edges or falling-edges of said dot clock pulses generated by changing a selection for a plurality of delayed-clock pulses, which are generated by delaying clock-pulses, outputted from a reference oscillator, in slightly different delay times, and

a controlling section to control a selecting operation for said plurality of delayed clock pulses, performed in said digital-delay dot clock adjusting section, so as to compensate for unevenness of scanning-light amount caused by an optical element employed in said optical-writing section; and

wherein said image-forming section performs an image-forming operation based on clock signals outputted from said digital-delay dot clock adjusting section.

8. An image-forming apparatus, comprising:

an image-forming section that includes an optical-writing section to form an image; and

a circuit for generating dot clock pulses for driving a light-emitting element employed in said optical-writing section included in said image-forming section;

wherein said circuit includes:

an index sensor to detect a light-beam, which is emitted from said light-emitting element and is deflected for scanning by a light-scanning device employed in said optical-writing section, and to output an index signal when said index sensor detects said light-beam at an end portion of a main-scanning region scanned by said light-beam;

a delay-chain section to generate a plurality of delayed-clock pulses by delaying clock-pulses, outputted from a reference oscillator, in slightly different delay times;

a synchronized clock pulse detecting section to select synchronized delayed-clock pulses, which are synchronized with said index signal, out of said plurality of delayed clock pulses generated in said delay-chain section, and to output a number of delay-stages, which is derived from said synchronized delayed-clock pulses, as synchronizing information;

a table memory to store scanning-light unevenness information, which represents unevenness of scanning-light amounts caused by an optical element employed in said optical-writing section;

a delayed-clock switching section to generate a select signal, for selecting a specific delayed-clock pulse, having a phase suitable for compensating for said unevenness of

scanning-light amount caused by said optical element employed in said optical-writing section, out of said plurality of delayed-clock pulses, based on said synchronized delayed-clock pulses and said synchronizing information outputted from said synchronized clock pulse detecting section and said scanning-light unevenness information stored in said table memory; and

a selector to select said specific delayed-clock pulse out of said plurality of delayed-clock pulses in response to said select signal generated by said delayed-clock switching section; and

wherein said image-forming section performs an image-forming operation based on clock signals outputted from said selector.

9. The image-forming apparatus of claim 8,

wherein said select signal is generated in said delayed-clock switching section by performing a calculating operation, based on said synchronized delayed-clock pulses outputted by said synchronized clock pulse detecting section and said scanning-light unevenness information stored in said table memory.

10. The image-forming apparatus of claim 8,

wherein said select signal is generated in said delayed-clock switching section by performing a table-converting operation, based on said synchronized delayed-clock pulses outputted by synchronized clock pulse detecting section and said scanning-light unevenness information stored in said table memory.

11. The image-forming apparatus of claim 8,

wherein said unevenness of scanning-light amount is a variation of light amount due to non-uniformity of reflectance and/or transmittance caused by said optical element.

12. The image-forming apparatus of claim 8,

wherein said delay-chain section, said synchronized clock pulse detecting section, said table memory and said selector are digital circuits fabricated in an integrated circuit.